

ECAP268 UNITS SELF-ASSESSMENT WITH ANSWERED

ECAP268 Unit 1 Self-Assessment 01

1. A unit of 8 bits is known as

- ☒ **A byte**
- ☐ A word
- ☐ A nibble
- ☐ A sentence

2. The hexadecimal number A is equivalent to _____ octal number.

- ☐ 9
- ☐ 10
- ☐ 11
- ☒ **12**

3. Which of the following symbol is not allowed in octal representation of numbers?

- ☒ **8**
- ☐ 7
- ☐ 6
- ☐ 5

4. Convert (47)₁₀ to binary representation.

- ☐ 110111
- ☒ **101111**
- ☐ 111011
- ☐ 111101

5. Convert (463)₁₀ to octal representation.

- ☒ **717**
- ☐ 177
- ☐ 616
- ☐ 166

6. Convert (7302)₁₀ to hexadecimal representation.

- ☐ 11286
- ☐ 68121
- ☐ 68C1
- ☒ **1C86**

7. Convert $(11101110)_2$ to decimal representation.

- ☐ 236
- ☐ 237
- ☒ **238**
- ☐ 239

8. Convert $(1010101011)_2$ to octal representation.

- ☐ 3521
- ☒ **1253**
- ☐ 3251
- ☐ 1235

9. Convert $(1010101011)_2$ to hexadecimal representation.

- ☒ **2AB**
- ☐ 21011
- ☐ BA2
- ☐ 11102

10. Convert $(43612)_8$ to decimal representation.

- ☐ 41381
- ☒ **18314**
- ☐ 478A
- ☐ A874

11. Convert $(13245)_8$ to binary representation.

- ☐ 1010010101101
- ☐ 1101110101101
- ☐ 1001101101101
- ☒ **1011010100101**

12. Convert $(65123)_8$ to hexadecimal representation.

- ☐ 35A6
- ☐ 35106
- ☒ **6A53**
- ☐ 61053

13. Convert $(BC4A)_{16}$ to decimal representation.

- ☐ 20284
- ☒ **48202**

- ☐ 1112410
- ☐ 1041211
- 14. Convert (A5F)₁₆ to binary representation.
 - ☒ **101001011111**
 - ☐ 111001011111
 - ☐ 110111011111
 - ☐ 111110100101
- 15. Convert (12345)₁₆ to octal representation.
 - ☐ 505122
 - ☒ **221505**
 - ☐ 122505
 - ☐ 212055
- 16. Find the 9's complement of 476005
 - ☒ **523994**
 - ☐ 523995
 - ☐ 499325
 - ☐ 599325
- 17. Find the 1's complement of 1010110
 - ☐ 0110001
 - ☐ 1010110
 - ☒ **0101001**
 - ☐ 1011000
- 18. Find the 10's complement of 321665
 - ☐ 678334
 - ☒ **678335**
 - ☐ 678333
 - ☐ None of these
- 19. Find the 2's complement of 1011111
 - ☐ 0100001
 - ☐ 0100010
 - ☒ **0100001**
 - ☐ 0100100

20. In fixed-point representation of numbers, the binary point is always fixed in which position.

- ☐ Extreme left
- ☐ Extreme right
- ☒ **Either Extreme Left or Extreme Right**
- ☐ None of the above

21. When the sign is represented by 0, then the integer binary number is

- ☒ **Positive**
- ☐ Negative
- ☐ 0
- ☐ Any of the above

22. What is the signed magnitude representation of -14

- ☒ **11110001**
- ☐ 11110010
- ☐ 10001110
- ☐ None of the above

ECAP268 Unit 2 Self-Assessment 02

1. $A+(B+C)=(A+B)+C$ is

- ☐ Commutative law
- ☒ **Associative law**
- ☐ Closure
- ☐ Distributive law

2. According to Annulment law, $A+1$ is equal to _____

- ☐ 0
- ☒ **1**
- ☐ A
- ☐ 2

3. Which term belongs to Idempotent law?

- ☒ **$A.A=A$**
- ☐ A. $(B+C) = A.B+A.C$
- ☐ $(A')'=A$
- ☐ $A+B=B+A$

4. $A(A+B)=A$ shows _____ law.

- ☐ Idempotent
- ☐ Annulment
- ☐ Distributive
- ☒ **Absorptive**

5. For evaluation of Boolean expressions, what will be order of?

1. AND
2. OR
3. NOT
4. Parentheses

- ☐ 1,2,3,4
- ☐ 2,1,4,3
- ☒ **4,3,1,2**
- ☐ None of the above

6. According to De-Morgan's theorem $(A+B)' = A' \cdot B'$, if $A=1$, $B=0$, then what is the output?

- ☐ 1
- ☒ **0**
- ☐ Either 1 or 0
- ☐ None of the above

7.

In a Boolean function, if there are n variables, then the number of combinations of 1s and 0s will be

- ☒ 2^n
- ☐ 2^{n+1}
- ☐ 2^{n-1}
- ☐ $2^{n+1}-2$

8. All boolean expressions regardless of their form can be converted to

- ☐ SOP
- ☐ POS
- ☒ **Both SOP and POS**
- ☐ None of the above

9. In which form, a single variable is allowed?

- ☐ SOP
- ☐ POS

- ☒ **Both SOP and POS**
 - ☐ None of the above
10. For 5 variables, the number of cells in a k-map will be
- ☐ 16
 - ☒ **32**
 - ☐ 64
 - ☐ 5
11. In 3 variable k-maps, which of the following is not adjacent to 011?
- ☒ **101**
 - ☐ 001
 - ☐ 111
 - ☐ 010
12. In 4 variable k-maps, which of the following is not adjacent to 0010?
- ☐ 0000
 - ☐ 0011
 - ☒ **0111**
 - ☐ 0110
13. Simplify the Boolean function, $A' + AB' + ABC'$
- ☐ $A + B + C$
 - ☒ **$A' + B' + C'$**
 - ☐ $A' + B + C$
 - ☐ $A' + B' + C$
14. After mapping of POS expression, for minimization we group together
- ☒ **0**
 - ☐ 1
 - ☐ Both 0 and 1
 - ☐ Either 0 or 1
15. After mapping of SOP expression, for minimization we group together
- ☐ 0
 - ☒ **1**
 - ☐ Both 0 and 1
 - ☐ Either 0 or 1

16. What is the other name of tabulation method which is used for simplification of Boolean expressions?

- ☒ **Quine McCluskey Method**
- ☐ K-map McCluskey Method
- ☐ Simplification McCluskey Method
- ☐ None of the above

17. What are the steps of simplification in tabulation method?

- ☐ Search for prime implicants
- ☐ Choosing of prime implicants for expression with least number of literals
- ☒ **Both searching of prime implicants and choosing of them for expression**
- ☐ None of the above

ECAP268 Unit 3 Self-Assessment 03

1. If $A=0$, $B=1$ and $C=0$, what will be the output in $(A \text{ OR } B) \text{ AND } C$?

- ☒ **0**
- ☐ 1
- ☐ 2
- ☐ None of the above

2. If $X=1$, $Y=1$ and $Z=1$ then what will be the output in $(X \text{ AND } Y) \text{ XOR } Z$?

- ☒ **0**
- ☐ 1
- ☐ 2
- ☐ None of the above

3. What will be the output, if two inputs, $R=0$ and $S=0$ are applied to XNOR logic.

- ☐ 0
- ☒ **1**
- ☐ 2
- ☐ None of the above

4. A combinational circuit that performs the addition of three bits is known as _____.

Full Adder

5. Which combinational circuit is represented by these Boolean expressions $S=x'y+xy'$, $C=xy$?

- ☐ Full Subtractor
- ☒ **Half Adder**
- ☐ Full Adder
- ☐ None of the above

6. When an overflow occurs, the sign is represented by _____ most bit in signed numbers.

- ☒ **Left**
- ☐ Right
- ☐ Middle
- ☐ None of the above

7. In case of full adder, if $X=1$, $Y=1$ and $Z=1$, then what will be the values of C and S ?

- ☐ 0, 0
- ☒ **1, 1**
- ☐ 0, 1
- ☐ 1, 0

8. A decimal adder requires a minimum of _____ inputs and _____ outputs.

- ☐ 9, 9
- ☐ 5, 9
- ☒ **9, 5**
- ☐ 5, 5

9. If we apply two BCD digits to a 4-bit binary adder. The adder will form the sum in binary and produces the result that ranges from ____ to ____.

- ☐ 0, 9
- ☐ 1, 9
- ☐ 1, 13
- ☒ **0, 19**

10. The addition of _____ to the binary sum converts it to the correct BCD representation and also produces an output carry as required.

- ☐ 0100
- ☐ 0101
- ☒ **0110**
- ☐ 0111

11.

Which of the following combinational circuit has 2^n inputs and n outputs?

- ☐ Adder
- ☐ Subtractor
- ☒ **Encoder**
- ☐ Decoder

12. In Octal to Binary encoder, we have 8 inputs and 3 outputs. At a particular time, how many inputs can be one?

- ☒ **1**
- ☐ 2
- ☐ 4
- ☐ 8

13. Which of the following combinational circuit has n inputs and 2^n outputs?

- ☐ Adder
- ☐ Subtractor
- ☐ Encoder
- ☒ **Decoder**

14. A decoder with enable input can function as a:

- ☐ Adder
- ☐ Subtractor
- ☐ Multiplexer
- ☒ **De-multiplexer**

15. Which of the following combinational circuit behaves as a data selector?

- ☐ Encoder
- ☐ Decoder
- ☒ **Multiplexer**
- ☐ Demultiplexer

16. Which of the following combinational circuit distributes the information taken from one line to a given number of output lines?

- ☐ Encoder
- ☐ Decoder
- ☐ Multiplexer

☒ **De-multiplexer**

17. In a demultiplexer, if we have only 1 input lines and 4 output lines, then how many selection lines will be there?

- ☐ 0
- ☐ 1
- ☒ 2
- ☐ 4

ECAP268 Unit 4 Self-Assessment 04

Top of Form

1. If the circuit requires the storage elements, then the circuit can be described in terms of

- ☒ **Sequential circuit**
- ☐ Combinational circuit
- ☐ Either sequential or combinational circuit
- ☐ Both sequential and combinational circuits

2. A flip-flop is a binary storage device which is capable of storing _____ bit of information.

- ☐ Zero
- ☒ **One**
- ☐ Two
- ☐ None of the above

3. Which of the following circuit use the clock signal as one of the input for synchronization?

- ☐ Asynchronous sequential circuit
- ☒ **Synchronous sequential circuit**
- ☐ Combinational circuit
- ☐ None of the above

4. A basic flip-flop circuit can be made up of

- ☐ Two NAND gates
- ☐ Two NOR gates
- ☒ **Either two NAND gates or two NOR gates**
- ☐ None of the above

5. In a basic flip flop circuit using NOR gates, what values of S and R describe the undefined condition?

- ☐ 0, 0
- ☐ 0, 1
- ☐ 1, 0
- ☒ **1, 1**

6. In a basic flip flop circuit using NAND gates, if $S=0$ and $R=0$ are provided, then what will be values of Q and Q' ?

- ☐ 0, 0
- ☐ 0, 1
- ☐ 1, 0
- ☒ 1, 1

7. In RS flip flop, when $CP=1$, $S=1$, and $R=0$, what do we call this state?

- ☒ Set state
- ☐ Reset state
- ☐ Memory state
- ☐ Invalid state

8. In D flip-flop, D input goes directly to _____ input and its complement goes to _____ input.

S, R

9. In D flip-flop, when $CP=1$ and $D=0$, the circuit will be in _____.

Clear sta

10. In a state table, which of these things are included?

- ☐ Present state, Input
- ☐ Next state, Output
- ☐ Present state and next state
- ☒ All present state, input, next state and output

11. A sequential circuit with m flip-flops and n inputs needs _____ rows in the state table.

- ☐ 2^m
- ☐ 2^n
- ☒ 2^{m+n}
- ☐ 2^{m-n}

12. In a state diagram, the states are represented by

- ☐ Rectangles
- ☐ Squares
- ☐ Lines
- ☒ Circles

13. When two states are equivalent, one of them can be removed without altering the input-output relationships. This statement is.

- ☒ True
- ☐ False

14. The complexity of the combinational circuit obtained depends on the binary state assignment chosen. This statement is

- ☒ True
- ☐ False

15. Which table lists the required inputs for a given change of state?
- ☐ Input table
 - ☐ Characteristic table
 - ☒ **Excitation table**
 - ☐ None of the above
16. In T flip-flop, if the value of T is 0, there will be no change in the next state. This statement is
- ☒ **True**
 - ☐ False
17. What will be the next state in T flip flop, if the value of T is 1.
- ☐ Same as the current state
 - ☒ **Complement of current state**
 - ☐ None of these
 - ☐ All of the above
18. During the design of combinational circuit part, the unused states are taken as
- ☐ 0
 - ☐ 1
 - ☒ **X**
 - ☐ None of the above
19. In applications which require the transfer the data, what kind of flip-flop is advisable to use?
- ☒ **D flip-flop**
 - ☐ T flip-flop
 - ☐ JK flip-flop
 - ☐ None of the above
20. A counter is self correcting, if by mistake the circuit goes to one of the unused state, the next count pulse transfers it to one of the valid states. This statement is
- ☒ **True**
 - ☐ False

ECAP268 Unit 5 Self-Assessment 05

1. The internal hardware organization of a digital computer is best defined by specifying:
- ☐ Set of registers
 - ☐ Sequence of micro-operations
 - ☐ A control to initiate the sequence of micro-operations
 - ☒ **All registers, sequence of micro-operations and a control for initializing**

2. Is it allowed to use the lower case letters for representation of computer registers?

- ☐ Yes ☒ **No**

3. The separation of two micro-operations is done using

- ☒ **Comma**
☐ Semi-colon
☐ Colon
☐ Asterisk

4. We can construct a common bus system for transferring of information between registers by using

- ☐ Multiplexers
☐ Three state bus buffers
☒ **Both multiplexers and three state bus buffers**
☐ None of the above

5. A three state gate exhibits

- ☐ Logic 0 state, logic 1 state and logic 2 state
☐ Logic 1 state, high-impedance state and logic 2 state
☒ **Logic 0 state, logic 1 state and high impedance state**
☐ None of the above

6. Which of the state behaves like an open circuit in three state gate?

- ☐ Logic 0
☐ Logic 1
☒ **High impedance state**
☐ None of the above

7. When the control input is _____, then the gate goes to high-impedance state.

- ☒ **0**
☐ 1
☐ 2
☐ 3

8. We can employ _____ to ensure that no more than one control input is active at any given time.

- ☐ Adder
☐ Multiplexer
☐ Demultiplexer
☒ **Decoder**

9. Which operation is defined in $R3 \leftarrow R1 + R2' + 1$

- ☐ Addition
- ☒ **Subtraction**
- ☐ Negation
- ☐ None of the above

10.

Which logical micro-operation is defined $F \leftarrow x \wedge y$

☐ OR ☒ AND ☐ XOR

11.

Which logical micro-operation is defined $F \leftarrow (x \oplus y)'$

☐ XOR ☒ XNOR ☐ NAND

12.

Which logical micro-operation is defined $F \leftarrow (x \wedge y)'$

- ☐ XOR
- ☐ XNOR
- ☒ **NAND**
- ☐ NOR

13. Apply selective clear on A, A=1010, B=1100 (logic operand)

- ☐ 1010
- ☐ 1100
- ☒ **0010**
- ☐ 0011

14. Apply selective complement on A, A=1010, B=1100 (logic operand)

- ☐ 1010
- ☒ **0110**
- ☐ 0011
- ☐ 1111

ECAP268 Unit 6 Self-Assessment 06

1. The computer reads each instruction from memory and places it in a _____ register.

- ☒ **Control**
- ☐ Processor
- ☐ Either control or processor
- ☐ None of the above

2. The computer reads each instruction from memory and places it in a _____ register.

- ☒ **Control**
- ☐ Processor
- ☐ Either control or processor
- ☐ None of the above

3.

The operation code must consist of atleast n bits for a given 2^n (or less) distinct operations.

- ☐ $n-1, 2^{n-1}$ ☒ $n, 2^n$ ☐ $n+1, 2^{n+1}$ ☐ None of the above

4. The instruction code format have two parts, the first part represents.

- ☒ **The operation to be performed**
- ☐ An address of operand
- ☐ Either operation or address
- ☐ None of the above

5. What is the total number of bits in an instruction?

- ☐ 8
- ☐ 12
- ☒ **16**
- ☐ 24

6. How many bits are used to distinguish between direct and indirect address?

- ☒ **1**
- ☐ 2
- ☐ 4
- ☐ 8

7. What is the total number of bits in PC?

☐ 8

☒ **12**

☐ 16

☐ None of the above

8. What is the total number of bits in TR?

☐ 8

☐ 12

☒ **16**

☐ None of the above

9. What is the total number of bits in TR?

☐ 8

☐ 12

☒ **16**

☐ None of the above

10. What is the total number of bits in OTR?

☒ **8**

☐ 12

☐ 16

☐ None of the above

11. Which of these register holds the address of instruction?

☒ **PC**

☐ AC

☐ AR

☐ DR

12. In a common bus system, how many registers just have LO input?

☐ 1

☒ **2**

☐ 3

☐ 4

13. A ____ bit sequence counter can count in binary from 0 to 15.

☐ 2

☒ **4**

☐ 6

☐ 8

14. Memory read/write cycle will be initiated with the _____ edge of a timing signal.

☐ Rising

15. During each instruction cycle, what is the next phase after decoding of instruction is

- ☐ Fetching of instruction from memory
- ☒ **Reading of effective address from memory**
- ☐ Execution of instruction
- ☐ None of the above

16. If D7=0, then what type of instruction it specifies?

- ☐ Register reference
- ☐ Input-output
- ☒ **Memory Reference**
- ☐ None of the above

17. If D7=1 and I=0, then what type of instruction it specifies?

- ☒ **Register reference**
- ☐ Input-output
- ☐ Memory Reference
- ☐ None of the above

18. If D7=1 and I=1, then what type of instruction it specifies?

- ☐ Register reference
- ☒ **Input-output**
- ☐ Memory Reference
- ☐ None of the above

ECAP268 Unit 7 Self-Assessment 07

1. In a basic computer, each instruction has a _____ letter symbol in programs.

- ☐ 2
- ☒ **3**
- ☐ 4
- ☐ 5

2. In a basic computer, each instruction has a _____ letter symbol in programs.

- ☐ 2 or A
- ☒ **3 or B**

☒ **4 or C**

☐ 5 or D

3. In BSA computer instruction, the hexadecimal code is

☐ 2 or A

☐ 3 or B

☐ 4 or C

☒ **5 or D**

4. In which category, the problem oriented symbols or formats are used?

☐ Binary code

☐ Octal/hexadecimal code

☐ Symbolic code

☒ **High level programming languages**

5. The fields, i.e., label, instruction and comment specify

☒ **Assembly language**

☐ High level programming language

☐ Octal programming language

☐ None of the above

6. A symbolic address must consist of _____ alphanumeric characters.

☐ 1

☐ 2

☐ 3

☒ **Either 1, 2 or 3**

7. The first character in the label field must be a

☒ **Letter**

☐ Numeral

☐ Symbol

☐ None of the above

8. A symbolic address in the label field is terminated by a _____ so that it will be recognized as a label by the assembler.

☒ **Comma**

☐ Semi-colon

☐ Dot

☐ Slash

9. A comment must be preceded by a _____ for the assembler to recognize the beginning of the comment field.

- ☐ Comma
- ☐ Semi-colon
- ☐ Dot
- ☒ **Slash**

10. The instruction CLA specifies

- ☒ **Non-MRI instruction**
- ☐ Direct address instruction
- ☐ Indirect address instruction
- ☐ None of the above

11. The pseudo-instruction ORG N gives the memory location for the instruction; here N is a _____ number.

- ☐ Decimal
- ☐ Binary
- ☐ Octal
- ☒ **Hexadecimal**

12. The translation into binary from the symbolic program is done by a special program called

- ☐ Linker
- ☒ **Assembler**
- ☐ Loader
- ☐ None of the above

13. The assignment of a memory location to each machine instruction and operand is done in _____ scan.

First

14. The address symbol table creation is done in _____ scan.

First

15. The table look up procedures is implemented in _____ pass.

Second

ECAP268 Unit 8 Self-Assessment 08

1. Which of the operation is not available as a machine instruction in basic computer?

- ☒ **OR**
- ☐ AND
- ☐ NOT

- ☐ None of the above
2. For arithmetic shift-left, it is necessary that the added bit in the least significant position should be _____.
☐ -1
☒ 0
☐ 1
☐ 2
3. Which of these instructions is considered as a logic operation that transfers a logic operand into the AC?
☒ **LOA**
☐ CMA
☐ AND
☐ CLA
4. Any logic function can be implemented using _____ and _____ operations.
☐ OR, XOR
☐ NOR, XNOR
☒ **AND, complement**
☐ OR, complement
5. CMA instruction is used for
☒ **Complementation**
☐ Accumulation
☐ Correlation
☐ None of the above
6. In the basic computer, the link between the main program and a subroutine is the _____ instruction.
☐ LDA
☒ **BSA**
☐ BAS
☐ None of the above
7. Which memory location of each subroutine serves as a link between the main program and the subroutine?
☒ **First**
☐ Second
☐ Fifth

- ☐ Last
8. Which instruction of the subroutine performs an operation commonly called subroutine return?
- ☐ First
 - ☐ Second
 - ☐ Fifth
 - ☒ **Last**
9. When computers have multiple processor registers then which register is usually employed to implement the subroutine linkage?
- ☒ **Index register**
 - ☐ Input register
 - ☐ Output Register
 - ☐ None of the above
10. The return to the main program after execution of subroutine is done by using _____
- ☒ **HLT**
 - ☐ Exit
 - ☐ Back
 - ☐ None of the above
11. Which of the instruction checks the input flag for the availability of character?
- ☒ **SKI**
 - ☐ INP
 - ☐ OUT
 - ☐ None of the above
12. A binary-coded character is transferred to the output device using _____ instruction?
- ☐ SKI
 - ☐ INP
 - ☒ **OUT**
 - ☐ None of the above
13. To turn the interrupt on, which instruction is used?
- ☐ INP
 - ☒ **ION**
 - ☐ IOF
 - ☐ None of the above

14. Interrupt sources can be used for

- ☐ Input transfers
- ☐ Output transfers
- ☐ Internal processing errors
- ☒ **All input and output transfers and internal processing errors**

15. A binary-coded character enters the computer using _____ instruction

- ☒ **INP**
- ☐ ION
- ☐ IOF
- ☐ None of the above

ECAP268 Unit 9 Self-Assessment 09

1. Which of the following component of CPU performs micro-operations?

- ☐ Control
- ☒ **ALU**
- ☐ Register set
- ☐ None of the above

2. The register that receives the information from the output bus is selected by the _____

- ☐ Encoder
- ☐ Multiplexer
- ☒ **Decoder**
- ☐ Demultiplexer

3. How many fields are included in a control word?

- ☐ 2
- ☐ 3
- ☒ **4**
- ☐ 5

4. Which of the following field is of 5 bits?

- ☐ SELA
- ☐ SELB
- ☐ SELD
- ☒ **OPR**

5. The fields SELA, SELB and SELD each consists of

- ☐ 2
- ☒ 3
- ☐ 4
- ☐ 5

6. A stack follows the rule of

- ☐ FIFO
- ☒ LIFO
- ☐ LILO
- ☐ None of the above

7. The register that holds the address for stack is called a _____

- ☒ Stack Pointer
- ☐ Stack Register
- ☐ Stack Pop
- ☐ Stack Push

8. The value of stack pointer always points towards the _____ of the stack

- ☐ Bottom
- ☐ Left
- ☐ Right
- ☒ Top

9. When we are removing any item from the stack, the content in SP will be

- ☐ Incremented
- ☒ Decrementd
- ☐ Remains same
- ☐ None of the above

10. When we are inserting any item to the stack, the content in SP will be

- ☒ Incremented
- ☐ Decrementd
- ☐ Remains same
- ☐ None of the above

11. The arithmetic expressions can be effectively calculated by _____ organization

- ☒ Stack
- ☐ Queue

- ☐ Graph
 - ☐ Tree
12. In polished notation, we place the operator is placed _____
- ☐ Between the operands
 - ☒ **Before the operands**
 - ☐ After the operands
 - ☐ The operator is not placed
13. Which of the following referred to as reverse polished notation?
- ☐ Infix notation
 - ☐ Prefix notation
 - ☒ **Postfix notation**
 - ☐ None of the above
14. The expression AB+ refers to as _____
- ☐ Infix notation expression
 - ☐ Prefix notation expression
 - ☒ **Postfix notation expression**
 - ☐ None of the above
15. Which of the following form is best suitable for stack manipulation?
- ☐ Polished notation
 - ☒ **Reverse Polished notation**
 - ☐ Accurate Polished notation
 - ☐ None of the above

ECAP268 Unit 10 Self-Assessment 10

1. Which of the following fields is a part of common instruction format?
- ☐ Operation field
 - ☐ Address field
 - ☐ Mode field
 - ☒ **All operation, address and mode fields**
2. The instruction ADD X represents
- ☒ **Single accumulator organization**
 - ☐ General register type organization

- ☐ Stack organization
 - ☐ None of the above
3. The instruction ADD R1, R2 represents
- ☐ Single accumulator organization
 - ☒ **General register type organization**
 - ☐ Stack organization
 - ☐ None of the above
4. In what kind of instruction, all operations are done between AC register and a memory operand?
- ☐ Three address instruction
 - ☐ Two address instruction
 - ☒ **One address instruction**
 - ☐ None of the above
5. In what kind of instruction, the address field is missing?
- ☐ Three address instruction
 - ☐ Two address instruction
 - ☐ One address instruction
 - ☒ **Zero address instruction**
6. Which instruction set is limited to the use of load and store instructions when communicating between memory and CPU?
- ☐ Two address instructions
 - ☐ One address instructions
 - ☐ Zero address instructions
 - ☒ **RISC instructions**
7. Which of the following organization have PUSH and POP instructions?
- ☐ Single accumulator organization
 - ☐ General register type organization
 - ☒ **Stack organization**
 - ☐ None of the above
8. What holds the address of the instruction to be executed next and is incremented each time an instruction is fetched from memory?
- ☒ **Program Counter**
 - ☐ Instruction Register
 - ☐ Input Register

- ☐ Output Register
9. Which of the following field is used to locate the operands needed for the operation?
- ☐ Address field
- ☒ **Mode field**
- ☐ Operation field
- ☐ None of the above
10. The complement accumulator represents
- ☒ **Implied mode**
- ☐ Immediate mode
- ☐ Register mode
- ☐ Relative address mode
11. In which mode, the operand is specified in the instruction itself?
- ☐ Implied mode
- ☒ **Immediate mode**
- ☐ Register mode
- ☐ Relative address mode
12. In indirect address mode, the effective address is calculated as:
- ☐ Effective address = address part of instruction / content of CPU register
- ☐ Effective address = address part of instruction * content of CPU register
- ☒ **Effective address = address part of instruction + content of CPU register**
- ☐ Effective address = address part of instruction - content of CPU register
13. In which addressing mode, the content of a base register is added to the address part of the instruction to obtain the effective address?
- ☐ Indexed addressing mode
- ☒ **Base register addressing mode**
- ☐ Relative addressing mode
- ☐ None of the above
14. Which of the following modes does not require any address field?
- ☐ Implied mode
- ☐ Immediate mode
- ☒ **Both immediate and implied mode**
- ☐ None of the above

15. All register reference instructions that use accumulator are _____ instructions.

- ☒ **Implied mode**
- ☐ Immediate mode
- ☐ Relative addressing mode
- ☐ None of the above

ECAP268 Unit 11 Self-Assessment 11

1. Why it is preferred to do parallel processing?

- ☐ For increasing the computer processing capabilities
- ☐ For increasing the throughput
- ☒ **For both increasing the throughput and processing capabilities**
- ☐ None of the above

2. Parallel processing can occur in

- ☐ Data stream
- ☐ Instruction stream
- ☒ **Both data and instruction stream**
- ☐ None of the above

3. In which group, all processors receive the same instruction from the control unit but operate on different items of data?

- ☐ SISD
- ☒ **SIMD**
- ☐ MISD
- ☐ MIMD

4. Of which group, as such there is no practical application. It is studied due to the theoretical interest?

- ☐ SISD
- ☐ SIMD
- ☒ **MISD**
- ☐ MIMD

5. In which group, the computer systems are capable of processing several programs at the same time?

- ☐ SISD
- ☐ SIMD

☐ MISD

☒ **MIMD**

6. Where can we apply the concept of pipeline organization?

☐ Arithmetic pipeline

☐ Instruction pipeline

☒ **Both arithmetic and instruction pipelines**

☐ None of the above

7. In which condition, the mantissa of the sum or difference is shifted right and the exponent incremented by one?

☒ **Overflow**

☐ Underflow

☐ Baseflow

☐ None of the above

8. In which condition, the number of leading zeros in the mantissa determines the number of left shifts in the mantissa and the number that must be subtracted from the exponent?

☐ Overflow

☒ **Underflow**

☐ Baseflow

☐ None of the above

9. The instruction fetch segment can be implemented by means of _____ buffer.

☒ **FIFO**

☐ LIFO

☐ FILO

☐ LILO

10. _____ occurs when an operand address cannot be calculated

☐ Data dependency

☒ **Address dependency**

☐ Calculation dependency

☐ None of the above

11. _____ occurs when an instruction needs data that are not available yet.

☐ Hardware interlocks

☐ Operand forwarding

☐ Delayed load

- ☒ **All hardware interlocks, operand forwarding and delayed load**
12. In _____ the control selects the target instruction if the condition is satisfied or the next sequential instruction if the condition is not satisfied.
- ☒ **Conditional branch**
- ☐ Unconditional branch
- ☐ Unconditional branch
- ☐ Unconditional branch
13. An _____ always alters the sequential program flow by loading the program counter with the target address.
- ☐ Conditional branch
- ☒ **Unconditional branch**
- ☐ Unconditional branch
- ☐ None of the above
14. Which of the following is a way for dealing with branching of instructions?
- ☐ Loop buffer
- ☐ Branch prediction
- ☐ Delayed branch
- ☒ **All loop buffer, branch prediction and delayed branch**

ECAP268 Unit 12 Self-Assessment 12

1. Which of the following is fastest kind of memory?
- ☐ Auxiliary memory
- ☒ **Cache memory**
- ☐ Main memory
- ☐ None of the above
2. Which of the following is slowest kind of memory?
- ☒ **Auxiliary memory**
- ☐ Cache memory
- ☐ Main memory
- ☐ None of the above
3. Magnetic tapes are a kind of
- ☒ **Auxiliary memory**
- ☐ Cache memory

- ☐ Main memory
 - ☐ None of the above
4. Which of the following memory does not deal directly with the CPU?
- ☒ **Auxiliary memory**
 - ☐ Cache memory
 - ☐ Main memory
 - ☐ None of the above
5. Which of the following memory is employed to compensate for speed differential between main memory access time and processor logic?
- ☐ Magnetic tapes
 - ☐ Magnetic disks
 - ☒ **Cache memory**
 - ☐ None of the above
6. In which of the following memory, the electric charges are applied to the capacitors?
- ☐ Static RAM
 - ☒ **Dynamic RAM**
 - ☐ Both static and dynamic RAMs
 - ☐ None of the above
7. The programs that are supposed to be stored permanently in the computer system are stored in
- ☐ RAM
 - ☒ **ROM**
 - ☐ Cache memory
 - ☐ Auxiliary memory
8. Which of the following memory is non volatile in nature?
- ☐ RAM
 - ☒ **ROM**
 - ☐ Both ROM and RAM
 - ☐ None of the above
9. As ROM can only read, so the data bus will always be in _____ mode
- ☐ Input
 - ☒ **Output**
 - ☐ Input/Output

- ☐ None of the above
- 10. Which of the following is an important characteristic of any device?
 - ☐ Access time
 - ☐ Transfer rate
 - ☐ Cost
 - ☒ **All access time, transfer rate and cost**
- 11. Memory space belongs to
 - ☐ Auxiliary memory
 - ☒ **Main memory**
 - ☐ Cache memory
 - ☐ None of the above
- 12. Address space belongs to
 - ☒ **Auxiliary memory**
 - ☐ Main memory
 - ☐ Cache memory
 - ☐ None of the above
- 13. Which of the following word is used to denote a block?
 - ☒ **Page frame**
 - ☐ Word frame
 - ☐ Line frame
 - ☐ Sentence frame
- 14. Which of the following is page replacement algorithm?
 - ☐ LRU
 - ☐ FIFO
 - ☒ **Both LRU and FIFO**
 - ☐ None of the above
- 15. Which of the following memory is accessed by content?
 - ☒ **Associative memory**
 - ☐ Auxiliary memory
 - ☐ Both associative and associative memories
 - ☐ None of the above
- 16. Which memory is placed between CPU and main memory?
 - ☒ **Cache memory**

- ☐ Associative memory
 - ☐ Random memory
 - ☐ None of the above
17. In which memory, no address is specified when writing?
- ☐ Cache memory
 - ☒ **Associative memory**
 - ☐ Random memory
 - ☐ None of the above
18. Which memory requires the logic circuit for matching the content?
- ☐ Cache memory
 - ☒ **Associative memory**
 - ☐ Random memory
 - ☐ Main memory
19. The access time of cache memory is _____ access time of main memory.
- ☐ Equal to
 - ☒ **Less than**
 - ☐ Greater than
 - ☐ None of the above

ECAP268 Unit 13 Self-Assessment 13

1. Which of the following control characters control the layout of printing?
- ☒ **Format effectors**
 - ☐ Information separators
 - ☐ Communication control characters
 - ☐ None of the above
2. Which of the following control characters separates the data into divisions like pages and paragraphs?
- ☐ Format effectors
 - ☒ **Information separators**
 - ☐ Communication control characters
 - ☐ None of the above

3. Which of the following control characters are used during the transmission of text between remote terminals?

- ☐ Format effectors
- ☐ Information separators
- ☒ **Communication control characters**
- ☐ None of the above

4. ASCII is a _____ bit code.

- ☐ 6
- ☒ **7**
- ☐ 8
- ☐ 9

5. Which of the following commands can be received by an interface?

- ☐ Control
- ☐ Status
- ☐ Data input and output
- ☒ **All control, status, data input and output**

6. Which of the following command is issued to activate the peripheral?

- ☒ **Control**
- ☐ Status
- ☐ Data input
- ☐ Data output

7. A _____ command causes the interface to respond by transferring data from the bus into one of its registers.

- ☐ Control
- ☐ Status
- ☐ Data input
- ☒ **Data output**

8. When interface receives an item of data from the peripheral and places it in its buffer register. Then what kind of command is issued?

- ☐ Control
- ☐ Status
- ☒ **Data input**
- ☐ Data output

9. If two units, such as CPU and I/O interface which are designed independently of each other and they share a private clock, then what mode of transfer is this?

- ☐ Synchronous mode
- ☒ **Asynchronous mode**
- ☐ Many-synchronous mode
- ☐ None of the above

10. If two units, such as CPU and I/O interface which are designed independently of each other and they share a common clock, then what mode of transfer is this?

- ☒ **Synchronous mode**
- ☐ Asynchronous mode
- ☐ Many-synchronous mode
- ☐ None of the above

11. In which method of data transfer, there is no way of knowing whether the other unit has actually placed or received the data?

- ☒ **Strobe method**
- ☐ Handshaking method
- ☐ Both strobe and handshaking methods
- ☐ None of the above

12. Which of the method provides a reply in the form of control signal to the unit that initiates the transfer?

- ☐ Strobe method
- ☒ **Handshaking method**
- ☐ Both strobe and handshaking methods
- ☐ None of the above

13. The line data valid in source initiated data transfer using handshaking is generated by__unit.

- ☒ **Source**
- ☐ Destination
- ☐ Either source or destination
- ☐ Both source and destination

14. Which of these is requires many wires for connection and is usually faster?

- ☒ **Parallel transmission**
- ☐ Serial transmission
- ☐ Equal transmission
- ☐ None of the above

15. In serial asynchronous transmission, the start bit is ____ and stop bit is ____.

- ☐ 1,1
- ☐ 0,0
- ☒ **0,1**
- ☐ 1,0

ECAP268 Unit 14 Self-Assessment 14

1. In verify logic, we have keywords.

- ☐ module
- ☐ endmodule
- ☒ **Both module and endmodule**
- ☐ None of the above

2. In verilog, how do we provide four bits input?

- ☒ **input [3:0] a;**
- ☐ input [0:3] a;
- ☐ input [0-3] a;
- ☐ input [3-0] a;

3. && represents

- ☐ Logical OR
- ☒ **Logical AND**
- ☐ All of the above
- ☐ None of the above

4. $X \wedge Y$ represents

- ☐ Bitwise AND
- ☐ Bitwise OR
- ☒ **Bitwise XOR**
- ☐ Bitwise XNOR

5. The conditional operator is defined by

- ☒ **?:**
- ☐ :?
- ☐ ?@
- ☐ @?

6. Which of the following is an HDL?

- ☐ Verilog
- ☐ VHDL
- ☒ **Both Verilog and VHDL**
- ☐ None of the above

7. The modulus operation is performed using

- ☐ +
- ☐ -
- ☒ %
- ☐ *

8. $\text{Out} = \sim X$, if $X=0$, then what will be the value of Out?

- ☐ 0
- ☒ **1**
- ☐ 2
- ☐ None of the above

9. This code represents
module abc (input a, output c);
assign c= \sim a;
endmodule

- ☒ **NOT gate**
- ☐ AND gate
- ☐ OR gate
- ☐ XOR gate

10. This code represents
module abc_gate (input a, input b, output c);
assign c= \sim (a | b);
endmodule

- ☒ **NOR gate**
- ☐ AND gate
- ☐ OR gate
- ☐ XOR gate

11. module abc_gate (input a, input b, output c);
assign c= \sim (a & b);
endmodule

- ☒ **NAND gate**

- ☐ AND gate
 - ☐ OR gate
 - ☐ XOR gate
12. module abc_gate (input a, input b, output c);
 assign c=~(a ^ b);
 endmodule
- ☐ NAND gate
 - ☐ AND gate
 - ☒ **XNOR gate**
 - ☐ XOR gate
13. module xyz(input logic a, b, output logic sum, carry);
 Assign sum =a^b, carry =a&b'
 endmodule
- ☒ **Half adder**
 - ☐ Full adder
 - ☐ Half Subtractor
 - ☐ Full Subtractor
14. module xyz (input logic S, i0, i1, output logic Z);
 assign Z=S?i0:i1
 endmodule
- ☐ Half adder
 - ☐ Full adder
 - ☒ **Multiplexer**
 - ☐ De-multiplexer
15. Which of these defines the capabilities of Verilog?
- ☐ Case sensitive
 - ☐ Vendor independence
 - ☒ **Both case sensitivity and independence from vendor**
 - ☐ None of the above